Claims after this response:

1(Currently Amended). A frequency divider comprising:

an input frequency divider for generating an intermediate signal having a frequency of f_i from an input signal having a frequency f_{in}, wherein $f_{in}=Rf_I$, R being an integer >1;

an edge counter that generates a value equal to the sum of the number of positive edges and the number of negative edges in said intermediate signal that have occurred since a reset signal was generated; and

an output generator that generates an output signal when said edge counter value reaches a value Q and generates said reset signal.

2(Currently Amended). A frequency divider comprising:

an input frequency divider for generating an intermediate signal having a frequency of f_i from an input signal having a frequency f_{in}, wherein $f_{in}=Rf_I$;

an edge counter that generates a value equal to the sum of the number of positive edges and the number of negative edges in said intermediate signal that have occurred since a reset signal was generated; and

an output generator that generates an output signal when said edge counter value reaches a value Q and generates said reset signal, wherein R=~~1~~2.

3(Previously presented). A frequency divider comprising:

an input frequency divider for generating an intermediate signal having a frequency of f_i from an input signal having a frequency f_{in}, wherein $f_{in}=Rf_I$, R being an integer >1;

an edge counter that generates a value equal to the number of edges in said intermediate signal that have occurred since a reset signal was generated; and

an output generator that generates an output signal when said edge counter value reaches a value Q and generates said reset signal;

wherein said edge counter comprises a positive edge counter that generates a positive count value equal to the number of positive going transitions in said intermediate signal since said reset signal; a negative edge counter that generates a negative count value equal to the number of negative going transitions in said intermediate signal since said reset signal; and an adder that generates the sum of said positive count and said negative count.

4(Original). The frequency divider of Claim 1 wherein said output generator further comprises a port for receiving a signal specifying Q.